

ARAB ACADEMY FOR SCIENCE, TECHNOLOGY AND MARITIME TRANSPORT College of Engineering and Technology

Electronics and Communications Engineering

Analysis and modeling of a Single-Electron Transistor (SET)

A Thesis Submitted in Partial Fulfillment to the Requirements for the Master's Degree in

Electronics and Communications Engineering

By

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Supervision

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AUGUST 2006



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Abstract

The wide range for applications for microelectronic devices is basically due to the scaling down of dimensions of such devices. Unfortunately, the scaling down and miniaturization of these devices is not infinite. There are some challenges and limitations for scaling down of these devices into the nanometer regime.

Accordingly, researchers are looking now to build new microelectronic devices with very small dimensions (nanotechnology). The behavior of such devices will be interpreted based on quantum mechanics principles due to small dimensions. The single-electron transistor (SET) is one of these devices which belongs to the quantum microelectronics family.

The thesis is organized as follows:

Chapter 1: The motivation behind searching for new electronic devices to be used in the nanometer regime, revision of the challenges facing conventional CMOS devices and revision of the promising nanotechnology devices.

Chapter 2: The promising applications for SET devices: hybrid, roomtemperature, logic and novel circuits.

Chapter 3: The physics and operation of the single-electron transistor (SET) including different theories used to describe the transport of electrons within the device and the Coulomb blockade phenomenon.

Chapter 4: The models used to simulate the SET including master equation method, Monte-Carlo method, SPICE models and computer programs used for each method.

Chapter 5: Our contribution of building a new fast and accurate model for SET devices using the reduced master equation method, also we will benchmark our results with that of "Quantum-Transport Group" at Delft university.

Chapter 6: Conclusions and proposed future work.

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Appendix : Our fast model code.

List of Symbols

Symbol	Description	Units
Å	Angstrom	
C_B	Capacitance of Back-Gate Capacitor in SET	F
C_D	Capacitance of Drain Tunnel Junction in SET	F
C_G	Capacitance of Gate Capacitor in SET	F
C_S	Capacitance of Source Tunnel Junction in SET	F
$D_f(E)$	The Density of States of the Final Side of the Potential	m ⁻³ J ⁻¹
	Barrier.	
$D_i(E)$	The Density of States on the Initial Side of the Potential	$m^{-3}J^{-1}$
	Barrier.	
Ε	Electric Field	V/m
Ε	Electron Charge	С
Ec	Charging Energy of Electron	eV
$E_{\rm c,f}$	The Conduction Band Edge of the Side where the Electrons is	eV
	Tunneling to.	
$E_{c,i}$	The Conduction Band Edge of the Side where the Electron	eV
	Resides Initially.	
E_f	Final Energy of a Tunneling Electron.	ev
E_i	Initial Energy of a Tunneling Electron.	ev
<i>f(E)</i>	Fermi-Dirac Distribution Which gives the Occupation	-
	Probability of Energy Levels in Equilibrium	
g _m	Transconductance	S
Н	Plank's Constant = 6.626E-34	Js
\overline{h}	Modified Plank's Constant = $h/2\pi = 1.055E-34$	Js
Ι	Current	Α
K	Constant Field Scaling Factor	-
K_B	Boltzman Constant = 1.381E-23	J/K
k i	Momentum of State i	Kg m/s
Ν	Number of Free Electrons	-
$P_i(t)$	Time Dependent Occupation Probability of State i	-
p_n	The Occupation Probability of the State n	-

Symbol	Description	Units
P _{th}	Threshold Probability	-
R_D	Resistance of Drain Tunnel Junction in SET	Ω
R_S	Resistance of Source Tunnel Junction in SET	Ω
R _T	Tunneling Resistance	Ω
T _{if}	Tunnel Transmission Coefficient from State <i>i</i> to a State <i>f</i>	-
V	Voltage	V
V _B	Back-Gate Voltage for SET	V
V _{DD}	Drain Bias Voltage for SET	V
V_G	Gate Voltage for SET	V
V _{th}	Threshold Voltage for SET	V
Z`	Total Capacitance of SET	F
$\Gamma_{i \to f}$	The Tunnel Rate from an Initial State <i>i</i> to a Final State <i>f</i> .	1/s
Γ_{ij}	Tunnel Rate From State j to State i	1/s
$\Gamma(n-1/n)$	The Tunneling Rate From State <i>n</i> to State <i>n-1</i>	1/s
ΔE	Quantum Level Spacing	eV
ΔF	Change in Free Energy in SET	eV
ΔV	The Voltage Difference across the Tunnel Junction.	V
τ	Tunnel Time	S

List of Acronyms

2-D	Two Dimensional
ASIC	Application Specific Integrated Circuit
BiCMOS	Bipolar CMOS
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal Oxide Semiconductor
<i>dna</i> SET	Deoxyribonucleic acid SET
DRAM	Dynamic Random Access Memory
FET	Field-Effect Transistors
ITRS	International Technology Roadmap for Semiconductors
KOSEC	Korea Single Electron Circuit Simulator
LTG	Linear Threshold Gate
MC	Monte-Carlo
ME	Master Equation
MIPS	Millions of Instructions per Second
MOS	Metal Oxide Semiconductor
MOSES	Monte-Carlo Simulator for Single-Electron Systems.
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
MPU	Microprocessor Unit
MTJ	Multiple-Tunnel Junction
nMOS	n-channel MOSFET
NRSC	National Radio Science Conference
NVM	Non-Volatile Memory
pMOS	p-channle MOSFET
QD	Quantum Dot
QT	Quantum Transport
rf	Radio Frequency
RNG	Random-Number Generator
SEM	Scanning Electron Microscopy
SENECA	Single Electron Nano-Electronic Circuit Analyzer
SET	Single-Electron Transistor
SIA	Semiconductor Industry Association

- SIMON SIMulation Of Nanostructures
- SoC System on Chip
- ssDNA Single-Stranded DNA
- STM Scanning Tunneling Microscope
- ULSI Ultra-Large Scale Integration

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